Abstract of the Disclosure

A chip-size semiconductor package includes a semiconductor chip; a metal pad formed on the semiconductor chip; a wafer coat formed over the semiconductor chip; a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern; a molding resin formed over the conductive wiring pattern; a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern; and a terminal which is formed on the molding resin and is connected to the conductive post. A connecting portion (boundary portion) of the conductive wiring pattern and conductive post is provided with a slit to disperse stress to be applied to the connecting portion.